FREQUENCY SHIFTING CIRCUIT AND METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to frequency shifting techniques suitable for a demodulator of a receiver in a multi-carrier communications system.

2. Description of the Related Art

In next generation mobile communications systems, much attention is focused on IMT-2000 (International Mobile Telecommunications-2000) system defined by ITU-R TG 8/1. There have been proposed several systems such as W-CDMA (Wideband-Code Division Multiple Access) and cdma2000, which may employ a multi-carrier scheme to allow high-speed data transmission.

The cdma2000 system is designed to realize upward compatibility with cdmaOne conforming to IS-95 and is likely to employ a multi-carrier scheme in downlink transmission. An example of the multi-carrier scheme in CDMA communications is shown in Fig. 10. In this example, it is assumed that the frequency offset of sub-carriers (Carrier-1 and Carrier+1) from the center carrier is 1.25 MHz and the chip rate is 1.2288 Mcps. In the cdmaOne communications, data can be transmitted at 14.4 kbps using a single carrier (center carrier). In contrast, the multi-carrier cdma system allows a maximum data rate of 43.2 kbps using three carriers.

To successfully receive such a multi-carrier signal, the simplest is to provide a different receiver dedicated to each of a plurality of carriers. However, the number of receivers to be needed increases as the number of carriers increases, resulting in increased amount of hardware and increased power consumption.

Another solution is that a single receiver is provided to receive signals on all the carriers and a digital baseband processor individually processes the received signals according to carrier frequencies. There have been proposed several methods for handling a received signal for each of a plurality of carriers.

In Japanese Patent Unexamined Publication No. 7-221806, a demodulator employing time division multiplexing scheme has been disclosed. More specifically, the respective carriers are identified by time slots of the time division multiplexing scheme and I- and Q-component signals for each carrier are frequency-shifted to produce baseband I- and Q-component signals for the center carrier by phase rotation computation.

In Japanese Patent Unexamined Publication No. 8-46654, a demodulator employing a carrier selection means at an input stage has been disclosed. More specifically, one of a plurality of carriers is selected according to carrier designation data. Only a signal of the selected carrier is subjected to quadrature frequency conversion to produce I- and Q-component signals and the I- and Q-component signals for each carrier are frequency-shifted to produce baseband I- and Q-component signals

for the center carrier by phase rotation computation.

In Japanese Patent Unexamined Publication No. 10-79718, a demodulator employing a Fast Fourier Transformer (FFT) for used in an OFDM (orthogonal frequency division multiplex) receiver has been disclosed. The FFT can be used to separate a plurality of carriers.

In the above prior arts, however, a ROM and a complex multiplier are needed for phase shifting and therefore there is disclosed no effective means for avoiding complication of the circuit, increase of the circuit scale, and increase of power consumption. A multi carrier receiver having a small circuit scale and saving power is not realized.

SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to provide a frequency shifting circuit and method suitable for a digital demodulator in a multi-carrier communications system.

Another object of the present invention is to provide a frequency shifting circuit and method suitable for a small-sized portable CDMA receiver.

According to an aspect of the present invention, a digital circuit for shifting a frequency band of a signal vector to a predetermined frequency band, wherein the signal vector is determined by a pair of I (in-phase) and Q (quadrature) components on I-Q plane, includes:

a control data generator for generating control data from a frequency difference between the frequency band and the predetermined frequency band; and

a signal vector rotator for rotating the signal vector on the I-Q plane by an angle determined depending on the control data to produce an output signal vector in the predetermined frequency band.

According to another aspect of the present invention, a digital circuit for shifting a plurality of frequency bands of input signal vectors to a predetermined center frequency band to produce an output signal vector for each frequency band, wherein each of the input signal vectors is determined by a pair of I (in-phase) and Q (quadrature) components on I-Q plane, includes:

an analog-to-digital converter for converting analog signal vectors to the input signal vectors according to a predetermined sampling clock;

a control data generator for generating control data from a frequency difference between each of the plurality of frequency bands and the predetermined center frequency band;

a signal vector rotator corresponding to each of the plurality of frequency bands, for rotating the input signal vectors on the I-Q plane by an angle determined depending on corresponding control data to shift the frequency bands of the input signal vectors to the predetermined center frequency band; and

a band-pass filter corresponding to the signal vector, for

receiving an output of the signal vector rotator and passing an output signal vector of the predetermined center frequency band.

The control data generator preferably includes a phase data generator for generating phase data Φ from the frequency difference in synchronization with the predetermined sampling clock, and a converter for converting the phase data Φ to the control data D consisting of a plurality of control bits D_k, where $-1 \leqq k \leqq m-2$ (m is a positive integer).

The phase data generator preferably generates the phase data Φ by computing an integral multiple of a unit angle Δ which is obtained from a frequency shift δ per period of the predetermined sampling clock, wherein the unit angle Δ is represented by $360^\circ \times \delta$, wherein the frequency shift δ is obtained by dividing the frequency difference by a frequency of the predetermined sampling clock and is represented in form of $RN / 2^m$ (RN is an rational number).

The converter preferably performs a conversion operation according to the following steps:

Step 1) $k = -1$ and $\Phi_k = \Phi$;

Step 2) D_k = sign bit of Φ_k;

Step 3) if $k = m - 2$, then exit, else go to step 4);

Step 4) $\Phi_{k+1} = \Phi_k - \theta_k$ when $D_k = 0$, and

$\Phi_{k+1} = \Phi_k + \theta_k$ when $D_k = 1$,

where $\theta_k = \arctan(2^{-k})$;

Step 5) $k = k + 1$; and

Step 6) go to step 3).

The signal vector rotator preferably includes a plurality of partial rotators R_k which are connected in series in descending order of a rotation angle, wherein the partial rotators R_k receive the control bits D_k, respectively, and each of the partial rotators R_k rotates an output of a previous stage R_{k-1} by a predetermined angle depending on a corresponding control bit received from the converter.

In the plurality of partial rotators, a first partial rotator R_{-1} rotates an input signal vector (I_{in} , Q_{in}) by an angle θ_{-1} to produce a first output signal vector ($I_{out,-1}$, $Q_{out,-1}$) as follows: $I_{out,-1} = D_{-1} \times Q_{in}$ and $Q_{out,-1} = -D_{-1} \times I_{in}$.

Further, each of partial rotators R_k ($0 \leq k \leq m-2$) rotates an input signal vector ($I_{in,k}$, $Q_{in,k}$) by an angle θ_k to produce an output signal vector ($I_{out,k}$, $Q_{out,k}$) as follows:

$$I_{out,k} = I_{in,k} + 2^{-k} \times D_k \times Q_{in,k} \text{ : and}$$

$$Q_{out,k} = -2^{-k} \times D_k \times I_{in,k} + Q_{in,k} ,$$

where D_k uses numerical value representation such that a numerical value "1" is represented by a logical value "1" and a numerical value "-1" is represented by a logical value "0".

The signal vector rotator rotates an input signal vector (I_{in}, Q_{in}) having an absolute value Z_{in} by an angle Θ while the absolute value Z_{in} becomes Z_{out}. where Θ and Z_{out} are represented as follows:

$$\Theta = D_{-1} \times 90° + \sum_{k=0}^{m-2} D_k \cdot \arctan(2^{-k}) \quad \textit{and}$$

$$Zout = \frac{Zin}{\prod_{k=0}^{m-2} \cos\theta_k}$$

Since a signal vector determined by the input I and Q components is rotated around the origin of the I-Q plane to be frequency-shifted to the center carrier band, the respective signal vectors of the frequency bands are obtained in the center carrier band.

Further, in multi carrier communications, especially in multi-carrier CDMA communications, the present invention can provide a frequency shifting circuit without the need of ROM and multiplier, which is simplified, reduced in power consumption, and suitable for a small-sized portable terminal. Since the frequency shifting circuit rotates a signal vector on the I-Q plane by means of digital computation, it is possible to demodulate received signals in the upper and lower bands into signals in the center band with extremely high precision.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing a circuit of a demodulation circuit employing a frequency shifting circuit according to an embodiment of the present invention;

FIG. 2 is a block diagram showing a phase accumulator used in the frequency shifting circuit of FIG. 1;

FIG. 3A is a block diagram showing a counter used in the phase accumulator of FIG. 2;

FIG. 3B is a timing chart showing a relationship between a sampling-rate clock and an output of the counter;

FIG. 4 is a block diagram showing a frequency shift control signal generator used in the frequency shifting circuit of FIG. 1;

FIG. 5 is a block diagram showing a de-rotator used in the frequency shifting circuit of FIG. 1;

FIG. 6 is a block diagram showing a rotator used in the frequency shifting circuit of FIG. 1;

FIG. 7 is a block diagram showing a partial rotation circuit used in the rotator and the de-rotator;

FIG. 8 is a block diagram showing an initial rotation circuit used in the rotator and the de-rotator;

FIG. 9 is a table showing correspondence between a partial rotation angle and its cosine in each stage of the partial rotation circuits in each of the rotator and the de-rotator; and

FIG. 10 is a schematic diagram showing an example of a power spectrum of a multi-carrier signal.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereafter, a preferred embodiment of the present invention will be described by referring to the drawings.

A frequency shifting demodulation circuit according to the present invention includes a well-known quadrature frequency converter (not shown) that reproduces In phase (I) components and Quadrature (Q) components from received signals according to the quadrature modulation scheme.

Here, it is assumed, as shown in Fig. 10, that the I and Q components are reproduced from received signals on the center carrier and the two sub-carriers. Frequencies of the sub-carriers are shifted from the center carrier by the same amounts in the lower-frequency and higher-frequency directions, respectively. In this example, the frequency offset of each sub-carrier is 1.25 MHz and the chip rate is 1.2288 Mcps. As described before, since the number of carriers is 3, a maximum data rate of 43.2 kbps can be obtained.

As shown in FIG. 1, the frequency shifting demodulation circuit further includes an analog-to-digital (A/D) converter 101 which causes the input I and Q components to be converted into digital form according to a sampling rate clock having a sampling rate which is eight times the chip rate. The A/D converter 101 outputs digital I and Q components to each of a de-rotator (or a negative frequency shifter) 102, a non-

rotator(or a non-shifter) 103, and a rotator(or a positive frequency shifter) 104. The de-rotator 102, the non-rotator 103, and the rotator 104 are connected to finite impulse response (FIR) filters 105, 106 and 107, respectively. The FIR filters 105, 106 and 107 have the same band-pass filtering characteristic for the center carrier Carrier-0 and output signals I_{-1} and Q_{-1} for higher sub carrier Carrier+1, signals I_0 and Q_0 for center carrier Carrier-0, and signals I_{+1} and Q_{+1} for lower sub-carrier Carrier-1 to corresponding despreaders (not shown), respectively. As described later, a phase accumulator 108 generates phase data Φ from a predetermined sampling rate clock and a frequency shift control signal generator 109 converts the phase data Φ to frequency shift control data D and outputs it to each of the de-rotator 102 and the rotator 104.

The de-rotator 102 decreases the frequency of I and Q components from the frequency of the sub-carrier Carrier+1 to the center carrier frequency band by rotating a signal point determined by the I and Q components for the sub-carrier Carrier+1 around the origin of an I-Q plane. Here, the amount of frequency shift is -1.25MHz. The non-rotator 103 does not shift the frequency of the center carrier but performs gain and timing compensation. The rotator 102 increases the frequency of I and Q components from the frequency of the sub-carrier Carrier-1 to the center carrier frequency band by rotating a signal point determined by the I and Q components for the sub-carrier Carrier-1. Here, the amount of frequency shift is +1.25MHz.

In this manner, the respective input signal vectors of the sub-carriers Carrier+1 and Carrier-1 are shifted to the frequency band of the center Carrier-0 and therefore the respective signal vectors (I_{+1} , Q_{+1}), (I_0 , Q_0), and (I_{-1} and Q_{-1}) are output through the FIR filters 105, 106 and 107 having same band-pass filtering characteristic for the center carrier Carrier 0.

Phase accumulator

Referring to FIG. 2, the phase accumulator 108 is composed of a sampling-rate clock generator 201, a counter 202, a full adder 203, and a register 204. As an example, the full adder 203 is a 13-bit full adder and the register 204 is a 13-bit register. A sampling rate clock generated by the sampling rate clock generator 201 is outputted to the counter 202 and the register 204 as well as the A/D converter 101. An integral multiple or a fraction of the sampling rate clock may be output to the counter 202 and the register 204. The counter 202 divides the sampling-rate clock in frequency by N (here, N-3) and outputs a carry signal W to the full adder 203. The full adder 203 adds the output of the register 204 received at input A, a predetermined binary number Z (here, Decimal 1041) received at input B, and the carry signal W received at input C. the 13-bit register 204 stores the output of the full adder 203 according to the sampling rate clock.

Hereinafter, the chip rate of each carrier is assumed to be 1.2288 Mcps. As for the sampling rate, it is assumed that

one chip is sampled by eight-times oversampling compared with the chip rate. Further, it is assumed that the frequency shift of each sub-carrier from the center carrier is 1.25 MHz. At this time, a frequency shift δ per sample is 1.25 MHz/(1.2288 Mchips/sec × 8 samples/chip), which is approximately 0.127/sample. Therefore, a product Δ of δ and 360 degrees is approximately 45.7 degrees. By taking Δ as a unit angle, phases in the range of 360 degrees ranging from -180 degrees to +180 degrees are represented by, for example, 13-bit binary numbers. In other words, 360 degrees are divided into 2^{13} (= 8192) parts. Thus, 2^{12} (= 4096) angle indication points are provided at equal intervals between -180 degrees and 0 degree, and 2^{12} (= 4096) angle indication points are provided at equal intervals between 0 degree and +180 degrees. Representing (Δ/360) approximately by using "2^{13}", we get (1041 + 2/3)/ 2^{13}). Converting the decimal number "1041" to a 13-bit binary number Z, we get "0 0100 0001 0001".

As shown in FIG. 2, the full adder 203 is supplied with an output of the 13-bit register 204 as its input A, and is further supplied with the above-described binary number Z, i.e., the decimal number 1041 (hereafter, simply referred to as "1041") as its input B. The full adder 203 adds the A input and the B input which is 1041. Thus, "A + 1041" is calculated. Further, to add the fraction 2/3 to the result "A + 1041", that is, to calculate "A + (1041 + 2/3)", the carry signal W output from the counter 202 is input to a carry terminal C of the full adder 203.

Eventually, the result of "A + (1041 + 2/3)" is output from the 13-bit register 204 as phase data Φ. The 13-bit register 204 holds the output of the full adder 203 at timing (e.g. leading edge) of the sampling-rate clock. In this way, the phase accumulator 108 produces phase data Φ as a binary number equal to the product of the unit angle △ and a natural number in synchronism with the sampling-rate clock.

Referring to FIG. 3A, the counter 202 is composed of two D-type flip-flop circuits 301 and 302 and an NOR gate 303. The output Q of the flip-flop circuit 301 is connected to the input D of the flip-flop circuit 302 and the one input of the NOR gate 303. The other input of the NOR gate 303 is connected to the output Q of the flip-flop circuit 302. The output of the NOR gate 303 is connected to the input D of the flip-flop circuit 301. The sampling-rate clock is supplied to both the clock terminals of the flip-flop circuits 301 and 302. The inverted output QB of the flip-flop circuit 302 is output as the carry signal W to the carry input C of the full adder 203. In this example, the counter 202 divides the frequency of the sampling-rate clock by N = 3.

As shown in Fig. 3B, the carry signal W, that is, the output of the counter 202 is "1" during two clock periods of the sampling-rate clock, and "0" during one clock period of the sampling-rate clock. Therefore, when the full adder 203 inputs the carry signal W at its carry input C from the count 202, 2 is added to (A + B) every three clock periods. As a result, 2/3 is added to the output of the full adder 203 per clock period.

Freq. shift control signal generator

Referring to FIG. 4, the frequency shift control signal generator 109 receives the phase data Φ from the phase accumulator 108, generates thirteen partial phases (Ψ_{-1}, Φ_0, Ψ_1, . . . , Ψ_{10}, Ψ_{11}) and thirteen control signals D (D_{-1}, D_0, D_1, . . . , D_{10}, D_{11}).

Hereafter, an algorithm for generating the control signals D on the basis of the phase data Φ will be described. In Fig. 4, functional blocks for implementing the algorithm are shown. The algorithm is constructed by the following steps:

Step 1) $k = -1$ and $\Phi_k = \Phi$;

Step 2) D_k = sign bit of Φ_k;

Step 3) if $k = 11$, then exit, else go to step 4);

Step 4) $\Psi_{k+1} = \Psi_k - \theta_k$ when $D_k = 0$, and

$\Phi_{k+1} = \Phi_k + \theta_k$ when $D_k = 1$;

Step 5) $k = k + 1$; and

Step 6) go to step 3).

More specifically, k is set to -1 and the phase Φ is set as Φ_{-1}. If Φ_{-1} has a positive value, then the most significant bit (MSB) D_{-1} of the control signal D is set to a logical value "1" and Ψ_0 is set to $\Phi_{-1} + 90$. If Ψ_{-1} has a negative value, then D_{-1} is set to a logical value "0" and Φ_0 is set to $\Phi_{-1} - 90$.

Subsequently, it is determined whether the numerical value Φ_0 obtained earlier is positive or negative. If Φ_0 has a positive value, then the logical value of D_0 is set to 1 and Φ

is set to $\Phi_0 + \theta_0$. If Φ_0 has a negative value, then D_0 is set to a logical value "0" and Φ_1 is set $\Phi_1 = \Phi_0 - \theta_0$, where $\theta_0 = \arctan(2^0)$. Generally, $\theta_k = \arctan(2^{-k})$.

In succession, it is determined whether Φ_1 is positive or negative. If Φ_1 has a positive value, then the logical value of D_1 is set to 1 and Φ_2 is set to $\Phi_1 + \theta_1$. If Φ_1 has a negative value, then D_1 is set to a logical value "0" and Φ_1 is set to $\Phi_1 - \theta_1$.

Here, θ_k to be added to or subtracted from Φ_k is supplied by twelve data selectors as indicated by reference numerals 401 to 404 depending on the sign bit of Φ_k, that is, Φ_k is positive or negative. If Φ_k is positive, then $-\theta k$ is supplied to a corresponding adder. When Φ_k is negative, then $+\theta k$ is supplied the corresponding adder. Generally, if D_k has a logical value "0", then $\Phi_{k+1} = \Phi_k - \theta_k$. If D_k has a logical value "1", then $\Phi_{k+1} = \Phi_k + \theta_k$.

By generating Φ_k in this manner, the numerical value of Φ_k can be brought closer to 0 successively as close as possible. There is improved the precision of approximation of the rotation angel Θ by which a signal vector in the I-Q plane is rotated. Generally, if the value of k becomes larger, then $\arctan(2^{-k})$ is assumed to be approximately 2 x $\arctan(2^{-k-1})$. Therefore, this method is more effective.

Rotator and De-rotator

Referring to FIG. 5, the rotator 104 is designed to rotate

a signal vector on the I-Q plane by an angle Θ determined depending on the control signals D (D_{-1}, D_0, D_1, ... , D_{10}, D_{11}). The rotator 104 is composed of thirteen partial rotation circuits (R_{-1}, R_0, R_1, R_{10}, R_{11}) which are cascade-connected. The respective control signals D_{-1}, D_0, D_1, ... , D_{10}, D_{11} are provided to the partial rotation circuits R_{-1}, R_0, R_1, ... , R_{10}, R_{11}.

Referring to FIG. 6, the de-rotator 102 is designed to rotate a signal vector on the I-Q plane by an angle of $-\Theta$ determined depending on the control signals D (D_{-1}, D_0, D_1, ... , D_{10}, D_{11}). The de-rotator 102 is composed of the same partial rotation circuits R_{-1}, R_0, R_1, ... , R_{10}, R_{11} as those used in the rotator 104 and inverters INV_{-1}, INV_0, INV_1, ... , INV_{10}, INV_{11}. The respective control signals D_{-1}, D_0, D_1, ... , D_{10}, D_{11} are connected to the partial rotation circuits R_{-1}, R_0, R_1, ... , R_{10}, R_{11} through the inverters INV_{-1}, INV_0, INV_1, ... , INV_{10}, INV_{11}.

Referring to FIG. 7, the partial rotation circuit R_{-1} at the initial stage receives the I_{in} and Q_{in} component signals from the A/D converter 101, and outputs $Q_{out,-1}$ and $I_{out,-1}$ component signals to the partial rotation circuit R_0 at the next stage.

The partial rotation circuit R_{-1} includes two multipliers 801 and 802, and a sign inverter 803. The Q_{in} component signal is input to the multiplier 801. The I_{in} component signal is input to the multiplier 802. The control signal D_{-1} is input to the sign inverter 803 and the multiplier 801. The sign inverter 803 supplies its output to the multiplier 802.

In other words, relations between inputs and outputs of the partial rotation circuit R_{-1} are represented by the following

equation (1):

$$I_{out,-1} = D_{-1} \times Q_{in} \quad \text{and}$$

$$Q_{out,-1} = -D_{-1} \times I_{in} \qquad (1),$$

where D_{-1} uses numerical value representation such that a numerical value "1" is represented by the logical value "1" and a numerical value "-1" is represented by the logical value "0".

The partial rotation circuit R_{-1} is a circuit for rotating the signal vector (I, Q) by an angle θ_{-1}. According to the equation (1), θ_{-1} is plus 90 degrees when the numerical value of the control signal D_{-1} is "-1" and θ_{-1} is minus 90 degrees when the numerical value of the control signal D_{-1} is "1". In this way, the partial rotation circuit R_{-1} rotates the signal vector without changing the absolute value of the signal vector.

Referring to FIG. 8, a partial rotation circuits R_k which is any of the partial rotation circuits R_0 to R_{11} is a circuit which receives $Q_{in,k}$ and $I_{in,k}$ from the previous stage and outputs $Q_{out,k}$ and $I_{out,k}$. The partial rotation circuit includes two constant multipliers 701 and 704, two multipliers 702 and 705, and two adders 703 and 706. The signal $I_{in,k}$ is input to the adder 703 and the constant multiplier 701. The output of the constant multiplier 701 is multiplied by a corresponding control signal Dk at the multiplier 702. The output of the multiplier 702 is inverted in sign and input to the adder 706. The signal $Q_{in,k}$ is input to the adder 706 and the constant multiplier 704. The output of the constant multiplier 704 is multiplied by a corresponding control signal Dk at the multiplier 705. The output of the multiplier 705 is input to the adder 703. In other

words, relations between inputs and outputs of each of the partial rotation circuits R_0 to R_{11} are represented by the following equation (2):

$$I_{out,k} = I_{in,k} + 2^{-k} \times D_k \times Q_{in,k} \quad \text{and}$$

$$Q_{out,k} = -2^{-k} \times D_k \times I_{in,k} + Q_{in,k} \qquad (2),$$

where D_k uses numerical value representation such that a numerical value "1" is represented by the logical value "1" and a numerical value "-1" is represented by the logical value "0".

The partial rotation circuit R_k (R_0 to R_{11}) is a circuit for rotating a signal vector ($Q_{in,k}$, $I_{in,k}$) by an angle θ_k. According to the above equation (2), θ_k is $+\arctan(2^{-k})$ degrees when the numerical value of the control signal D_k is "-1" and θ_k is $-\arctan(2^{-k})$ degrees when the numerical value of the control signal D_k is "1". In this way, each of the partial rotation circuits R_0 to R_{11} rotates the input signal vector ($Q_{in,k}$, $I_{in,k}$) by the angle θ_k. As a result of the rotation, the absolute value $Z_{in,k}$ of the input signal vector becomes proportionate to the reciprocal of $\cos\theta_k$. Therefore, the absolute value $Z_{out,k}$ of the output signal vector becomes ($Z_{in}/\cos\theta_k$).

Heretofore, the partial rotation circuits have been described. The rotator 104 is a circuit formed by cascade-connecting thirteen partial rotation circuits (R_{-1}, R_0, R_1, ..., R_{10}, R_{11}). When a signal vector (I, Q) having an absolute value Z_{in} is input to the rotator 104, the signal vector is rotated by an angle Θ and its absolute value becomes Z_{out} to output it from the rotator 104. The angle Θ and Z_{out} are represented by the following equations (3) and (4).

$$\Theta = D_{-1} \times 90^{\circ} + \sum_{k=0}^{11} D_k \cdot \arctan(2^{-k}) \quad \cdots \quad (3)$$

$$Zout = \frac{Zin}{\prod_{k=0}^{11} \cos\theta_k} \quad \cdots \quad (4)$$

FIG. 9 is a table showing correspondence relations among k, 2^{-k}, θ_k, $\cos\theta_k$, and 45×2^{-k}. According to the table, the denominator of the right side of the equation (4) is a constant 0.6072529591.

As described above, in multi-carrier communications, in particular, multi-carrier CDMA communications, the present invention heretofore described provides a frequency shifting circuit which is simplified, reduced in power consumption, and suitable for a small-sized portable terminal. Since the frequency shifting circuit rotates a signal vector on the I Q plane by means of digital computation, it is possible to demodulate received signals in the upper and lower bands into signals in the center band with extremely high precision.